Capacity Development and skills Enhancement Activity

AWARENESS OF TRENDS IN TECHNOLOGY

WORKSHOP ON RECENT TRENDS IN VLSI DESIGN

ECE - Seminar Events

Website : www.rgcetpdy.ac.in

RAJIV GANDHI COLLEGE OF ENGINEERING AND TECHNOLOGY

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(Sponsored by Sri Balaji Educational and Charitable Public Trust)
Pondy - Cuddalore Main Road, Kirumampakkam, Puducherry - 607 403.

27.02.2019

From

P. Tamilselvan,
Assistant Professor (Stage II),
Department of ECE,
Rajiv Gandhi College of Engineering and Technology,
Kirumampakkam,
Puducherry - 607 403.

To

The Principal,
Rajiv Gandhi College of Engineering and Technology,
Kirumampakkam,
Puducherry - 607 403.

THROUGH THE HEAD OF THE DEPARTMENT, DEPARTMENT OF ECE

Respected Sir,

Sub: - Request for permission to conduct a Two days workshop on "Recent Trends in VLSI Design" for IV Year ECE Students-reg.

We have planned to conduct a two day's workshop on the topic "Recent Trends in VLSI Design"on 01/03/2019 & 02/03/2019. I will be in-charge of the workshop. The aforementioned workshop will be offered to the IV Year / VIII Semester students of the ECE Department.

I kindly request you to grant permission to conduct this program. Enclosed are the details of the workshop for your perusal and approval.

Thanking you,

Yours sincerely,

P. Tamilselvan
Event Incharge

Forwarded to Principal

B. S. L.

RAJIV GANDHI COLLEGE OF ENGINEERING & TECHNOLOGY * Department of ECE * Puducherry

Dr. E. VIJAYAKRISHNA RAPAKA
B.Tech. (Mech.), M.Tech.(Energy), Ph.D. (IIT Madras)
M.I.S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I.,
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

No: RGCET/ECE/Circular/2018-19/45 Date: 22.02.2019

CIRCULAR

We are excited to inform you that a two-day workshop on **"Recent Trends in VLSI Design"** from 01.03.2019 – 02.03.2019, is organized exclusively for our IV Year students This workshop is designed to provide both theoretical knowledge and practical skills essential for mastering these advanced VLSI Technologies.

Resource Person Details:

Mr.A.D.Senthilkumar ,Senior Verification Engineer and

Mr.A.Robert Jean, Senior Design Engineer, Vistronics Design Solutions, Chennai

Venue: Seminar Hall

All are invited

B. S
HOD / ECE

Copy to:

1. The Principal
2. Circulate to all Faculty Members and ECE students
3. Notice board / file

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M.I.S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I.,
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(NAAC ACCREDITED WITH GRADE A)
Pondy - Cuddalore Main Road, Kirumambakkam, Pondicherry - 607 403.

The HOD, Staff and Students of

E C E

IETE STUDENTS FORUM (ISF)

Department cordially invite you to the inauguration of

IETE Sponsored Two Days National Level Workshop on

"Recent Trends in VLSI Design"

On Friday, 1st March 2019 at 9.45 a.m

in the Seminar Hall

Shri M. K. RAJAGOPALAN
Chairman
Sri Balaji Educational & Charitable Public Trust
will preside over the function

Mr. A.D.SENTHILKUMAR
(Senior Verification Engineer) &
Mr. A.ROBERT JEAN
(Senior Design Engineer)
Vistronics Design Solutions
Chennai
will be the Chief Guests and address the gathering

Dr. E. VIJAYAKRISHNA RAPAKA
Principal, RGCET
will felicitate

Dr. K. AYYAPPAN
Vice-Principal, RGCET
will honor

Mrs. B. SHOBA
HOD, ECE
will welcome the gathering

Dr. E. VIJAYAKRISHNA RAPAKA
B.Tech. (Mech.), M.Tech.(Energy), Ph.D. (IIT Madras)
M.I.S.T.E., F.I.I.P.E., M.C.S.I M.C.I.I.,
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Report : Workshop on Recent Trends in VLSI Design

Name of the Department	Department of Electronics and Communication
Name of the Event Organized	Workshop on Recent Trends in VLSI Design
Date of the Event Organized	01/03/2019 & 02/03/2019
Time	9.00 am – 4.00 pm
No. of participants	63
Name of the Chief Guest / Speakers	Mr.A.D.Senthilkumar ,Senior Verification Engineer and Mr.A.Robert Jean, Senior Design Engineer, Vistronics Design Solutions, Chennai
Venue	Seminar Hall, Administrative Block

Seminar Objectives:

1. Provide participants with an understanding of advanced VLSI design concepts and techniques.
2. Explore emerging trends such as low-power design, hardware security, and neuromorphic computing.
3. Foster hands-on learning through practical exercises or case studies.
4. Facilitate networking and knowledge sharing among participants and industry experts.

Seminar Schedule:

Date	Time	Topics covered
01/03/19	9.30 am – 11.30 am	Fundamentals and Advanced Techniques – Introduction to VLSI Design
	11.30 am – 11.45am	Tea Break
	11.45 am – 1.00 pm	Advanced CMoS Technologies
	1.00 pm – 1.45 pm	Lunch Break
	1.45 pm – 2.45 pm	Low power Design Techniques
	2.45 pm – 3.00 pm	Tea Break
	3.00 pm – 4.00 pm	High Speed Design and Signal Integrity
02/03/19	9.30 am – 11.30 am	Emerging Trends and Practical Applications – Hardware Security
	11.30 am – 11.45am	Tea Break
	11.45 am – 1.00 pm	Neuromorphic Computing
	1.00 pm – 1.45 pm	Lunch Break
	1.45 pm – 2.45 pm	Quantum Computing and VLSI
	2.45 pm – 3.00 pm	Tea Break
	3.00 pm – 4.00 pm	Case Studies

RAJIV GANDHI COLLEGE OF ENGINEERING & TECHNOLOGY Department ECE

Dr. E. VIJAYAKRISHNA RAPAKA
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The two-day workshop conducted on the topic "Recent Trends in VLSI Design", was held on March 01/03/2019& 02/03/2019. The speakers for the workshopwere invited from industry Vistronics Design Solutions, Chennai. The workshop was aimed at providing ECE students with basic essential knowledge like essentials of Verilog HDL Programming Concepts, covering both basic and advanced functionalities and to equip them with practical skills for VLSI applications. Moreover,industrial simulation tools that are used for design and development of real time projects was also discussed as case study. The workshop was designed to cover various aspects of Digital Concepts, from understanding different types modeling concepts in Verilog HDL.

The target participant for the workshop was Final Year ECE department students. A total of 63 students attended the workshop.

EventIncharge

Mr. P. Tamilselvan
Assistant Professor(Stage II),
Department of ECE
Rajiv Gandhi College of Engineering and Technology
Date:02/03/2019

Head of the Department

HEAD OF THE DEPARTMENT
Electronics and Communication Engg
Rajiv Gandhi College of Engineering & Tech

RAJIV GANDHI COLLEGE OF ENGINEERING & TECHNOLOGY
Department of ECE
Puducherry

Dr. E. VIJAYAKRISHNA RAPAKA
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List of Students Attended **Academic Year: 2018-19**

Name of the Program: Recent Trends in VLSI Design

S.No	Register Number	Name	Year /Sem	Department
1	14TC0407	ALAM HUSSAIN	IV/VIII	ECE
2	15TC0501	AISWARYA M	IV/VIII	ECE
3	15TC0503	AMANULLAH N	IV/VIII	ECE
4	15TC0504	AMRUTHA P	IV/VIII	ECE
5	15TC0505	ANAGA MALINI S	IV/VIII	ECE
6	15TC0506	ANBARASAN K	IV/VIII	ECE
7	15TC0507	ARTHI H	IV/VIII	ECE
8	15TC0508	ARUN RATHNARAJ P	IV/VIII	ECE
9	15TC0509	BABY ANILAA R	IV/VIII	ECE
10	15TC0510	BOOPITHA V	IV/VIII	ECE
11	15TC0511	DHANAPRIYA K	IV/VIII	ECE
12	15TC0512	DIVYA J	IV/VIII	ECE
13	15TC0513	GAYATHRI V	IV/VIII	ECE
14	15TC0514	GIRIDHARAN R	IV/VIII	ECE
15	15TC0515	GURU ARAVINDHAN S	IV/VIII	ECE
16	15TC0516	HARISH KUMAR M	IV/VIII	ECE
17	15TC0517	HEMAPRIYA K	IV/VIII	ECE
18	15TC0518	JENCY SAGAYARANI A	IV/VIII	ECE
19	15TC0519	JEYASEELAN K	IV/VIII	ECE

Dr. E. VEERA[illegible]
B.Tech. (Mech., [illegible] (Madras)
[illegible]
PRINCIPAL
Rajiv Gandhi College of Engineering & Technology
Pondy - Cuddalore Main Road,
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Department of ECE

S.No	Register Number	Name	Year /Sem	Department
20	15TC0520	KABILAN P	IV/VIII	ECE
21	15TC0521	KALPANA J	IV/VIII	ECE
22	15TC0522	KARTHIK R	IV/VIII	ECE
23	15TC0523	KARTHIKA R	IV/VIII	ECE
24	15TC0524	KARTHIKEYAN S	IV/VIII	ECE
25	15TC0525	MANIMEGALAI N	IV/VIII	ECE
26	15TC0526	MANIKANDAN D	IV/VIII	ECE
27	15TC0527	MANIKANDAN N	IV/VIII	ECE
28	15TC0528	MARTINA AGNES DEVAKIRUBAI T	IV/VIII	ECE
29	15TC0530	MOHAMMED AZARUDEEN J	IV/VIII	ECE
30	15TC0531	MOHANRAJ V	IV/VIII	ECE
31	15TC0533	NIRMAL KUMAR R	IV/VIII	ECE
32	15TC0535	PARTHIBAN R	IV/VIII	ECE
33	15TC0536	PAVITHRA K	IV/VIII	ECE
34	15TC0538	PRADHEEP S	IV/VIII	ECE
35	15TC0539	PREETHA P	IV/VIII	ECE
36	15TC0540	PREETHI M	IV/VIII	ECE
37	15TC0541	PREETHI R	IV/VIII	ECE
38	15TC0543	PRIYADHARSHINI J	IV/VIII	ECE

Dr. E. VIJAYAKRISHNA RAPAKA
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Department of ECE

S.No	Register Number	Name	Year /Sem	Department
39	15TC0544	PRIYANKA L	IV/VIII	ECE
40	15TC0545	PRIYANKA. V	IV/VIII	ECE
41	15TC0547	RAJESHWARI S	IV/VIII	ECE
42	15TC0548	RASHMI R	IV/VIII	ECE
43	15TC0549	RATHINAMURUGAN D	IV/VIII	ECE
44	15TC0550	RAVICHANDRAN N	IV/VIII	ECE
45	15TC0551	REGINA D	IV/VIII	ECE
46	15TC0553	SAKTHI BALAJI P	IV/VIII	ECE
47	15TC0554	SANMUGA PRIYA M	IV/VIII	ECE
48	15TC0555	SANTHA KUMAR R S	IV/VIII	ECE
49	15TC0556	SASIREKHA P	IV/VIII	ECE
50	15TC0557	SOUMYA TAZE R	IV/VIII	ECE
51	15TC0558	SOWMIYA S	IV/VIII	ECE
52	15TC0560	SRUDHI R	IV/VIII	ECE
53	15TC0562	SUSHMITHAA S	IV/VIII	ECE
54	15TC0564	THIRUSELVAM K	IV/VIII	ECE
55	15TC0565	THIRUVARASAN S	IV/VIII	ECE
56	15TC0566	UDAYAKUMAR R	IV/VIII	ECE
57	15TC0567	VAITHEESHWARAN I	IV/VIII	ECE

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S.No	Register Number	Name	Year /Sem	Department
58	15TC0568	VASANTHVELAN J	IV/VIII	ECE
59	15TC0569	VENKATESH A	IV/VIII	ECE
60	15TC0570	VENKATESH S	IV/VIII	ECE
61	15TC0571	VIJAYABHARATHI K	IV/VIII	ECE
62	15TC0572	YUDHASITH R	IV/VIII	ECE
63	15TC0573	YUVASRI S	IV/VIII	ECE
Total Enrolled Students			**63**	

Event Incharge

Head of the Department

HEAD OF THE DEPARTMENT
Electronics And Communication Engg
Rajiv Gandhi College of Engg. & Tech
PUDUCHERRY - 607 402

RAJIV GANDHI COLLEGE OF ENGINEERING & TECHNOLOGY * Puducherry * Department of ECE

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Attendance Sheet **Year / Semester: IV/VIII** **Academic Year: 2018-19**

Name of the Program: Recent Trends in VLSI Design

S.No	Register Number	Name	01/03/2019	02/03/2019
1	14TC0407	ALAM HUSSAIN	P	P
2	15TC0501	AISWARYA M	P	P
3	15TC0503	AMANULLAH N	P	P
4	15TC0504	AMRUTHA P	P	P
5	15TC0505	ANAGA MALINI S	P	P
6	15TC0506	ANBARASAN K	P	P
7	15TC0507	ARTHI H	P	P
8	15TC0508	ARUN RATHNARAJ P	P	P
9	15TC0509	BABY ANILAA R	P	P
10	15TC0510	BOOPITHA V	P	P
11	15TC0511	DHANAPRIYA K	P	P
12	15TC0512	DIVYA J	P	P
13	15TC0513	GAYATHRI V	P	P
14	15TC0514	GIRIDHARAN R	P	P
15	15TC0515	GURU ARAVINDHAN S	P	P
16	15TC0516	HARISH KUMAR M	A	P
17	15TC0517	HEMAPRIYA K	P	P
18	15TC0518	JENCY SAGAYARANI A	P	P
19	15TC0519	JEYASEELAN K	P	P
20	15TC0520	KABILAN P	P	P
21	15TC0521	KALPANA J	P	P
22	15TC0522	KARTHIK R	P	P
23	15TC0523	KARTHIKA R	P	A

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S.No	Register Number	Name	01/03/2019	02/03/2019
24	15TC0524	KARTHIKEYAN S	P	P
25	15TC0525	MANIMEGALAI N	P	P
26	15TC0526	MANIKANDAN D	P	P
27	15TC0527	MANIKANDAN N	P	P
28	15TC0528	MARTINA AGNES DEVAKIRUBAI T	P	P
29	15TC0530	MOHAMMED AZARUDEEN J	P	P
30	15TC0531	MOHANRAJ V	A	P
31	15TC0533	NIRMAL KUMAR R	P	P
32	15TC0535	PARTHIBAN R	P	P
33	15TC0536	PAVITHRA K	P	P
34	15TC0538	PRADHEEP S	P	P
35	15TC0539	PREETHA P	P	P
36	15TC0540	PREETHI M	P	P
37	15TC0541	PREETHI R	P	P
38	15TC0543	PRIYADHARSHINI J	P	P
39	15TC0544	PRIYANKA L	P	P
40	15TC0545	PRIYANKA. V	P	P
41	15TC0547	RAJESHWARI S	P	P
42	15TC0548	RASHMI R	P	P
43	15TC0549	RATHINAMURUGAN D	P	P
44	15TC0550	RAVICHANDRAN N	P	P
45	15TC0551	REGINA D	P	P
46	15TC0553	SAKTHI BALAJI P	P	A
47	15TC0554	SANMUGA PRIYA M	P	P

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S.No	Register Number	Name	01/03/2019	02/03/2019
48	15TC0555	SANTHA KUMAR R S	P	P
49	15TC0556	SASIREKHA P	P	P
50	15TC0557	SOUMYA TAZE R	P	P
51	15TC0558	SOWMIYA S	P	P
52	15TC0560	SRUDHI R	P	P
53	15TC0562	SUSHMITHAA S	P	P
54	15TC0564	THIRUSELVAM K	P	P
55	15TC0565	THIRUVARASAN S	P	P
56	15TC0566	UDAYAKUMAR R	P	P
57	15TC0567	VAITHEESHWARAN I	P	P
58	15TC0568	VASANTHVELAN J	P	P
59	15TC0569	VENKATESH A	P	P
60	15TC0570	VENKATESH S	P	P
61	15TC0571	VIJAYABHARATHI K	P	P
62	15TC0572	YUDHASITH R	A	P
63	15TC0573	YUVASRI S	P	P
Total Number of Students			63	63
Total Students Absent			3	2
Total Students Present			60	61

Event Incharge

Head of the Department

Dr. E. VIJAYAKRISHNA RAPAKA
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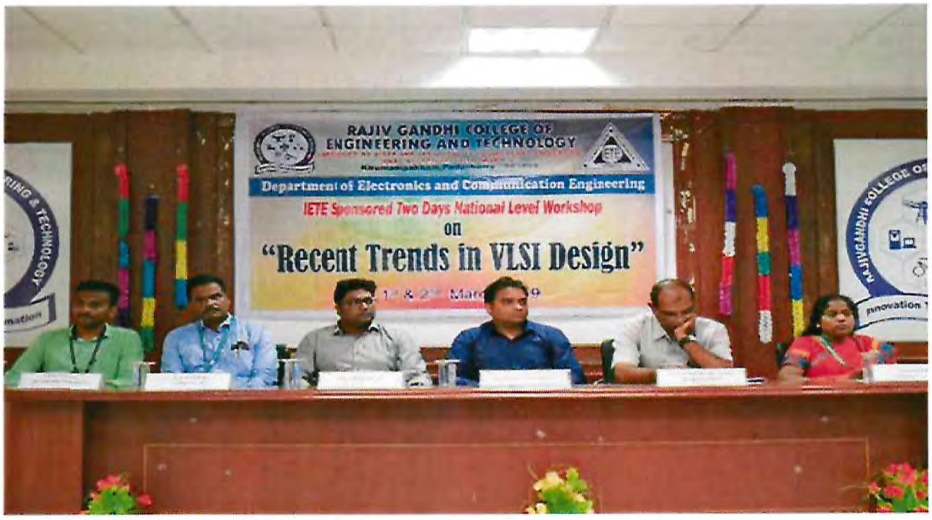
RAJIV GANDHI COLLEGE OF ENGINEERING & TECHNOLOGY
Department of ECE
Puducherry

Workshop Photos:



IETE Sponsored two days National level workshop on Recent Trends in VLSI Design with the Chief Guests Mr.A.D.Senthilkumar and Mr.A.Robert Jean from Vistronics Design Solutions, Chennai

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FEEDBACK FORM

Workship Tittle.....

Date: ..... Venue:.....

Name:.....

Register Number: .....Semester/Year: .....

THE DESIGN OF THE COURSE

A. **Were objectives of the workshop clear to you?** Y / N
B. **The workshop contents met with your expectations**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
C. **The lecture sequence was well planned**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
D. **The contents were illustrated with adequate examples**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
E. **The level of the workshop was too high**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
F. **The workshop contents compared with your expectations was too theoretical**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
G. **The workshop exposed you to new knowledge and practices**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

THE CONDUCT OF THE COURSE

A. **The lectures were clear and easy to understand**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
B. **The teaching aids were effectively used**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
C. **The workshop material handed out was adequate**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
D. **The instructors encouraged interaction and were helpful**
   1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree
E. **Were objectives of the course realized?** Y / N
F. **Please give overall rating of the workshop**

90% - 100% ( ) 60% - 70% ( )

80% - 90% ( ) 50% - 60% ( )

70% - 80% ( ) below 50% ( ) **Signature**

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Multiple Choice Questions:

Name:----------

Department/Sec:

Workshop Title:

1. VLSI technology uses _____ to form integrated circuit.
a) transistors
b) switches
c) diodes
d) buffers

2. Medium scale integration has _____
a) ten logic gates
b) fifty logic gates
c) hundred logic gates
d) thousands logic gates

3. The difficulty in achieving high doping concentration leads to _____
a) error in concentration
b) error in variation
c) error in doping
d) distribution error

4. _____ is used to deal with effect of variation.
a) chip level technique
b) logic level technique
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d) system level technique

5. As die size shrinks, the complexity of making the photomasks _____
a) increases
b) decreases
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d) cannot be determined

6. _____ architecture is used to design VLSI.
a) system on a device
b) single open circuit
c) system on a chip
d) system on a circuit

7. Which is the high level representation of VLSI design?
a) problem statement
b) logic design
c) HDL program
d) functional design

8. _____ is used in logic design of VLSI.
a) LIFO
b) FIFO
c) FILO
d) LILO

9. Which provides higher integration density?
a) switch transistor logic
b) transistor buffer logic
c) transistor transistor logic
d) circuit level logic

10. Physical and electrical specification is given in _____
a) architectural design
b) logic design
c) system design
d) functional design

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Signature

Answers:

1.a
2.c
3.b
4.d
5. a
6. c
7. a
8. b
9.c
10.d

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Department of Electronics and Communication Engineering

FEEDBACK FORM

Workship Tittle: Recent Trends in VSLI Design.

Date: 2/3/2019 Venue: Seminar Hall

Name: Sushmithaa. S

Register Number: 15TC0562 Semester/Year: 4 Yr. / 8 Sem.

THE DESIGN OF THE COURSE

A. **Were objectives of the workshop clear to you?** ~~Y~~ / N

B. **The workshop contents met with your expectations**
1. Strongly disagree 2. Disagree 3. Neutral ~~4.~~ Agree 5. Strongly agree

C. **The lecture sequence was well planned**
1. Strongly disagree 2. Disagree ~~3.~~ Neutral 4. Agree 5. Strongly agree

D. **The contents were illustrated with adequate examples**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree ~~5.~~ Strongly agree

E. **The level of the workshop was too high**
1. Strongly disagree 2. Disagree 3. Neutral ~~4.~~ Agree 5. Strongly agree

F. **The workshop contents compared with your expectations was too theoretical**
1. Strongly disagree 2. Disagree ~~3.~~ Neutral 4. Agree 5. Strongly agree

G. **The workshop exposed you to new knowledge and practices**
1. Strongly disagree 2. Disagree 3. Neutral ~~4.~~ Agree 5. Strongly agree

THE CONDUCT OF THE COURSE

A. **The lectures were clear and easy to understand**
1. Strongly disagree 2. Disagree 3. Neutral ~~4.~~ Agree 5. Strongly agree

B. **The teaching aids were effectively used**
1. Strongly disagree 2. Disagree ~~3.~~ Neutral 4. Agree 5. Strongly agree

C. **The workshop material handed out was adequate**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree ~~5.~~ Strongly agree

D. **The instructors encouraged interaction and were helpful**
1. Strongly disagree 2. Disagree 3. Neutral ~~4.~~ Agree 5. Strongly agree

E. **Were objectives of the course realized?** ~~Y~~ / N

F. **Please give overall rating of the workshop**

90% - 100% ( ) 60% - 70% (✓)

80% - 90% ( ) 50% - 60% ( )

70% - 80% ( ) below 50% ( )

Sushmithaa.

Signature

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FEEDBACK FORM

Workship Tittle... Recent trends in VLSI Design.....

Date: ....02/03/2019..... Venue:.....Seminar Hall.....

Name:.....Hema priya.K.....

Register Number: ...15TC051F...Semester/Year: .....IV/VIII th Sem.....

THE DESIGN OF THE COURSE

A. Were objectives of the workshop clear to you? Y / N

B. The workshop contents met with your expectations
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

C. The lecture sequence was well planned
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

D. The contents were illustrated with adequate examples
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

E. The level of the workshop was too high
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

F. The workshop contents compared with your expectations was too theoretical
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

G. The workshop exposed you to new knowledge and practices
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

THE CONDUCT OF THE COURSE

A. The lectures were clear and easy to understand
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

B. The teaching aids were effectively used
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

C. The workshop material handed out was adequate
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

D. The instructors encouraged interaction and were helpful
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

E. Were objectives of the course realized? Y / N

F. Please give overall rating of the workshop

90% - 100% ( ) 60% - 70% ( )

80% - 90% ( ) 50% - 60% ( )

70% - 80% ( ) below 50% ( )

Hema priya.

Signature

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FEEDBACK FORM

Workship Tittle...Recent trend in VLSI Design.....

Date: ...02/03/2019..... Venue:....Seminar hall.....

Name:...Vasanthvelan J.....

Register Number: ..15TC0568.....Semester/Year: .....IV/VIII.....

THE DESIGN OF THE COURSE

A. **Were objectives of the workshop clear to you?** Y / N

B. **The workshop contents met with your expectations**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

C. **The lecture sequence was well planned**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

D. **The contents were illustrated with adequate examples**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

E. **The level of the workshop was too high**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

F. **The workshop contents compared with your expectations was too theoretical**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

G. **The workshop exposed you to new knowledge and practices**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

THE CONDUCT OF THE COURSE

A. **The lectures were clear and easy to understand**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

B. **The teaching aids were effectively used**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

C. **The workshop material handed out was adequate**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

D. **The instructors encouraged interaction and were helpful**
1. Strongly disagree 2. Disagree 3. Neutral 4. Agree 5. Strongly agree

E. **Were objectives of the course realized?** Y / N

F. **Please give overall rating of the workshop**

90% - 100% ( ) 60% - 70% ( )

80% - 90% (✓) 50% - 60% ( )

70% - 80% ( ) below 50% ( )

Signature

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Multiple Choice Questions:

Name: Sushmitaaa.S
15TCD562
Department/Sec: ECE

Workshop Title: Recent Trends in VSLI Design

1. VLSI technology uses _____ to form integrated circuit.
a) transistors
b) switches
c) diodes
d) buffers

2. Medium scale integration has _____
a) ten logic gates
b) fifty logic gates
c) hundred logic gates
d) thousands logic gates

3. The difficulty in achieving high doping concentration leads to _____
a) error in concentration
b) error in variation
c) error in doping
d) distribution error

4. _____ is used to deal with effect of variation.
a) chip level technique
b) logic level technique
c) switch level technique
d) system level technique

5. As die size shrinks, the complexity of making the photomasks _____
a) increases
b) decreases
c) remains the same
d) cannot be determined

6. _____ architecture is used to design VLSI.
a) system on a device
b) single open circuit
c) system on a chip
d) system on a circuit

7. Which is the high level representation of VLSI design?
a) problem statement
b) logic design
c) HDL program
d) functional design

8. _____ is used in logic design of VLSI.
a) LIFO
b) FIFO
c) FILO
d) LILO

9. Which provides higher integration density?
a) switch transistor logic
b) transistor buffer logic
c) transistor transistor logic
d) circuit level logic

10. Physical and electrical specification is given in _____
a) architectural design
b) logic design
c) system design
d) functional design

Sushmitaaa
Signature

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Multiple Choice Questions:

Name: Hema priya.K
15TC0517
Department/Sec: ECE

Workshop Title:

1. VLSI technology uses _____ to form integrated circuit.
a) transistors
b) switches
c) diodes
d) buffers

2. Medium scale integration has _____
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d) functional design

Hemapriya
Signature

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Department of Electronics and Communication Engineering

Multiple Choice Questions:

Name: Vasanthvelan J (15TC0568)

Department/Sec: ECE

Workshop Title: Recent trends in VLSI Design

1. VLSI technology uses _____ to form integrated circuit.
a) transistors
b) switches
c) diodes
d) buffers

2. Medium scale integration has _____
a) ten logic gates
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